WHAT IS CLAIMED IS:

1. A semiconductor device manufacturing method comprising the steps of:

a) forming at least one conductive layer pattern on a substrate, thereby forming a resulting structure;

b) forming an interlayer insulating layer on the resulting structure;

c) exposing contact regions between the conductive layer patterns; and

d) after the step c), forming an insulating spacer on sidewalls of the conductive layer patterns.

2. The method of claim 1, wherein the interlayer insulating layer is formed of a material having a dielectric constant less than 3.5.

3. The method of claim 2, wherein in step b), the interlayer insulating layer is formed of an oxide layer.

4. The method of claim 3, where in step c), the interlayer insulating layer is etched with a gas mixture including Ar, C, and F.

5. The method of claim 4, wherein in step c), the interlayer insulating layer is etched at a pressure of 1 mTorr to 100 mTorr.

6. A method of claim 1, after step b), further comprising a step of:

b1) forming a mask pattern covering a top portion of the conductive layer patterns, wherein the mask pattern is formed of a layer selected from a group consisting of a silicon

nitride layer, a silicon oxy-nitride layer, and an oxide layer.

7. The method of claim 2, wherein in step b), the interlayer insulating layer is formed of a polymer.

8. The method of claim 7, wherein in step c), the interlayer insulating layer is etched by using a gas selected from Ar, O_2, N_2, H_2, CH_4, C_2H_4, and C_xF_y.

9. The method of claim 8, wherein in step c), the interlayer insulating layer is etched at a pressure of 1 mTorr to 100 mTorr.

10. The method of claim 2, the step c) comprising:

C1) providing an etching mask, wherein a contact hole pattern selected from a group consisting of a straight line shape, T-shape, and I-shape is defined; and

C2) etching the interlayer insulating layer with the etching mask.

11. A semiconductor device manufacturing method comprising the steps of:

a) forming conductive layer patterns on a substrate, forming a resulting structure;

b) forming an interlayer insulating layer on the resulting structure; and

c) exposing contact regions between the conductive layer patterns, by selectively etching the interlayer insulating layer, and at the same time, forming a spacer by leaving the interlayer insulating layer on sidewalls of the conductive layer patterns.

12. The method of claim 11, wherein the interlayer insulating layer is formed with a material having a dielectric constant less than 3.5.

13. The method of claim 12, wherein in step b), the interlayer insulating layer is formed of an oxide layer.

14. The method of claim 13, where in step c), the interlayer insulating layer is etched with a gas mixture including Ar, C, and F.

15. The method of claim 14, wherein in the step c), the interlayer insulating layer is etched at a pressure of 1 mTorr to 100 mTorr.

16. A method of claim 11, after step b), further comprising a step of:

b1) forming a mask pattern covering a top portion of the conductive layer pattern, wherein the mask pattern is formed of a layer selected from the group consisting of a silicon nitride layer, a silicon oxy-nitride layer, and an oxide layer.

17. The method of claim 12, wherein in step b), the interlayer insulating layer is formed of a polymer.

18. The method of claim 17, wherein in step c), the interlayer insulating layer is etched by using a gas selected from Ar, O_2, N_2, H_2, CH_4, C_2H_4, and C_xF_y.

19. The method of claim 18, wherein in step c), the interlayer insulating layer is etched at a pressure of 1 mTorr to 100 mTorr.

20. The method of claim 12, the step c) comprising:

C1) providing an etching mask, wherein a contact hole pattern selected from the group consisting of a straight line shape, T-shape, and L-shape is defined; and

C2) etching the interlayer insulating layer with the etching mask.